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Antennas Embedded in CMOS Integrated Circuits

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Abstract: In this work we propose novel integrated antennas for chip-to-chip wireless interconnects. In order to save chip area, the available CMOS circuit ground planes can be used as radiating elements. The interference between the integrated antennas and the on-chip circuit interconnects should be minimised. This can be obtained by introducing a transformer in the antenna feeding network.

Keywords: Integrated on-chip antennas, wireless chip-to-chip communication, antenna feeding, electromagnetic interference.

1 Introduction

THE chip-to-chip communication rate is limited by the cross-talk and the dispersion in wired interconnects. It is possible to increase the communication rate is to use advanced coding techniques [1]. Wireless links can also be considered an alternative, as they can provide higher data rates at short distances. Additional advantage of the wireless chip-to-chip networks is the considerable simplification of the system design, as the number of the required on-board connection wires is reduced [2]. RF fr4ont-end circuits in CMOS technology are available in literature [3], so the problem of on-chip antenna integration remains to be solved. Antennas integrated on a silicon substrate have been investigated in literature [4–6], but they require additional chip area.

In order to save chip area we propose to use the same on-chip structures both for antenna electrodes and for electronic circuit elements. This can be obtained by cutting into patches the top-most CMOS metallisation layer, which is used as a circuit ground plane, and use this patches as antenna electrodes. An inductive

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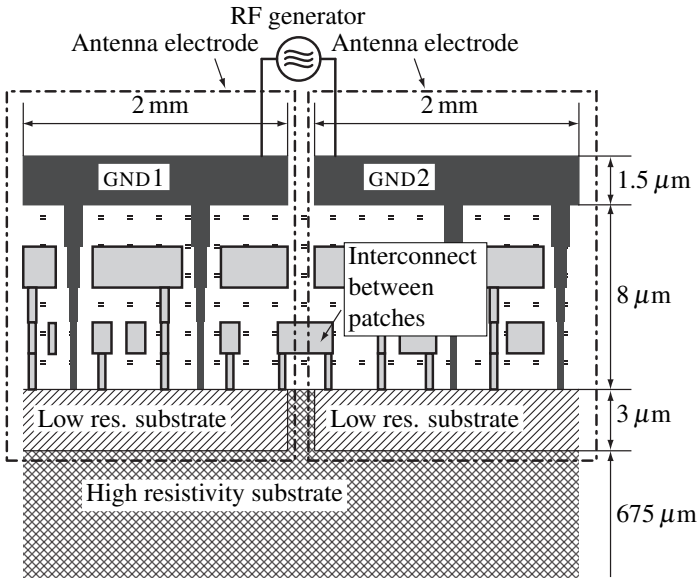

Fig. 1: Cross-section view of integrated on-chip antenna, using the ground planes as antenna electrodes. The separated areas of the ground planes have to be connected to each other using inductive connections. The RF generator is also integrated in the CMOS circuit. Figure is no to scale.

coupling between the ground planes is required, which provides low-impedance contact between the patched for the CMOS operational frequencies and a high-impedance contact for the antenna currents.

2 Antenna Description Characteristics

A cross-section of a CMOS integrated circuit is shown in Fig.1. The integrated circuit is manufactured on a silicon substrate. In order to minimise the integrated antenna losses, the substrate needs to be of high resistivity, say 1000 Ωcm or more. The substrate thickness is 675 μm. The CMOS technology requires higher substrate conductivity, so a thin layer of low-impedance silicon is manufactured on top of the high-impedance substrate. In this layer of thickness about 3 μm the active elements are manufactured. Several metallisation layers of total thickness of 8 μm follow, which contain the CMOS interconnects. The CMOS ground plane is manufactured in the top-most metallization layer. This ground plane is cut into patches and an RF voltage is impress across the gap between the patches. As the total current on the two patches will be unequal zero, the patches will be excited in antenna mode and will radiate.

Various patch configurations and excitations are possible depending on the desired antenna resonance frequency and directional pattern. For example the rectan-

gular ground plane can be cut in a 2×2 rectangular patches (Fig. 2). An RF generator can be connected to the diagonal set of patches, exciting them in an antenna mode. A second antenna mode can be excited with another generator, connected to the remaining patch pair, as shown in Fig. 2a. Thus two antennas for a 2×2 MIMO channel can be integrated on-chip without any chip area sacrifice. It is also possible to introduce the RF generators across the adjacent patches in the same patch configuration, as shown in Fig. 2b. Again two different antenna modes are excited.

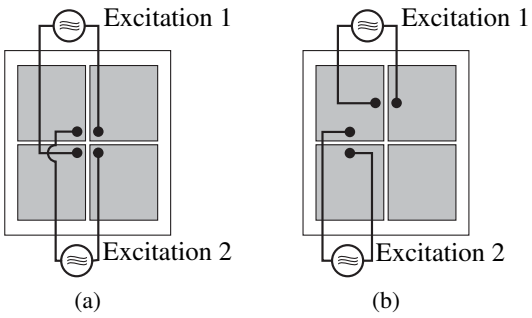

Fig. 2: Diagonal (a) and adjacent (b) antenna excitation.

In both cases described above the coupling between the antennas can not be neglected. It can be shown, though, that if properly accounted for, this coupling does not degrade the MIMO channel capacity [7].

In order to verify the radiation properties of the described antenna structures, a scaled prototyped was manufactured under the assumption that the CMOS interconnects do not influence the antenna. As a benchmark case a diagonally excited 2×2 patch configuration, as shown in Fig. 3, has been studied. Antennas with patch dimensions $m \times n = 20$ mm^2 have been manufactured on a RO4350B$^{\text{TM}}$ substrate with $\varepsilon_r = 3.48$. The gaps between all patches are 100 μm wide. The antennas were placed at a distance $d = 35$ mm apart. A comparison between the simulated and measured antenna return loss and channel gain is presented in Fig. 4.

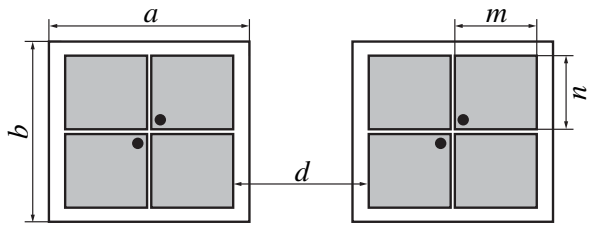

Fig. 3: Dimensions of the simulated and manufactured scaled antenna prototypes. Excitation points are marked.

Figure 5 shows the simulated current distribution of the manufactured antenna.

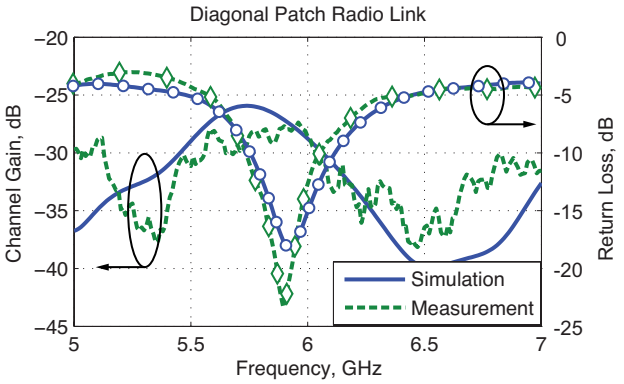

Fig. 4: Simulated and measured antenna return loss and channel gain of the configuration, presented in Fig. 3.

This figure gives insight into the operating mode of the antenna. The slot between the patches forms a transmission line, terminated with the RF generator in the middle of the antenna, and with an open circuit at the antenna edge. Thus a standing

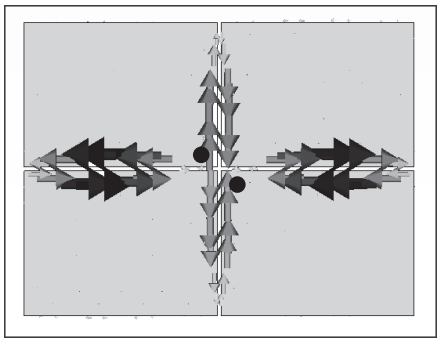

Fig. 5: Surface current distribution at f = 6 GHz of the 2×2 patch structure from Fig. 3. Excitation points are marked.

wave pattern is formed in the slot, which is responsible for the radiation properties of the antenna. The wavelength λ_g in the slot transmission line, formed between the patches, is given by

$$\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}} \tag{1}$$

where λ_0 is the free-space wavelength. The effective dielectric constant $\varepsilon_{eff} = \sqrt{(\varepsilon_r + 1)/2}$, ε_r being the dielectric permittivity of the substrate, accounts for the fact that the electric field spreads over both the substrate and the free space. So the resonant frequency of the 15mm long gap (see Fig. 3) is 6.68 GHz. The resonant

frequency of the 20 mm long gap is 5.01 GHz. The resonant frequency of the manufactured antenna is about 5.9 GHz, which, as expected, is between the resonant frequencies of the gaps.

3 The Influence of the Interconnects

In the previous discussion the influence of the interconnects has been neglected. This assumption can be justified for interconnects, located underneath the patches [8], but not for the interconnects across the gap between the patches. As discussed in the previous section, the antenna electric field is mostly concentrated in the gap between the patches, therefore introduction of conductors in the gap will perturb the standing wave pattern and thus the antenna resonance frequency and input impedance will be changed. Since the cross-patch interconnects are parallel to the antenna electric field (see Fig.6), RF current will be induced in the interconnects, thus increasing the bit error probability of the CMOS circuitry underneath the antenna.

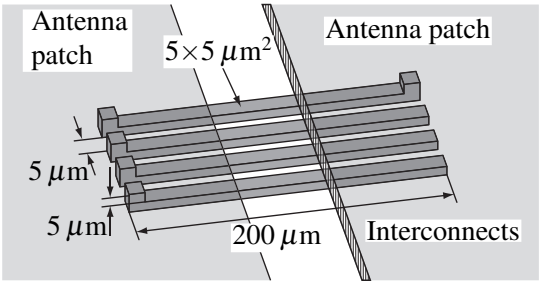

Fig. 6: A 4-wire interconnection bus across the gap between the patches.

In order to investigate the influence of the interconnect a two-patch antenna has been optimised for a resonance frequency of 66 GHz (Fig.7). The influence of the interconnects on the antenna return loss is shown in Fig.8.

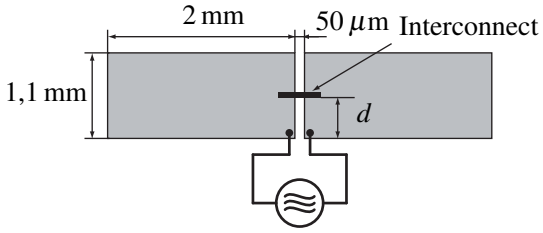

Fig. 7: Top view of a double-patch antenna, operating at 66 GHz.

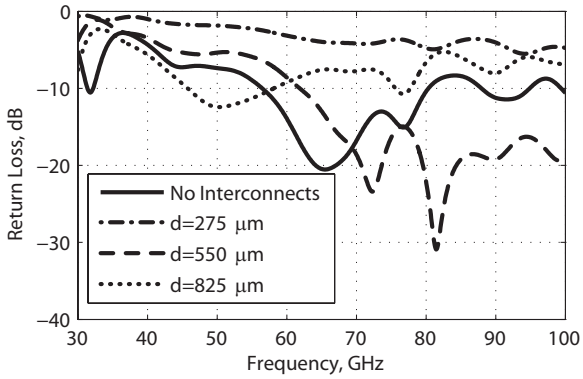

Fig. 8: Influence on the reflection loss of an integrated antenna of a single line, connecting the areas between the two patches.

Figure 9 compares the antenna electric filed in the presence and in the absence of interconnects.

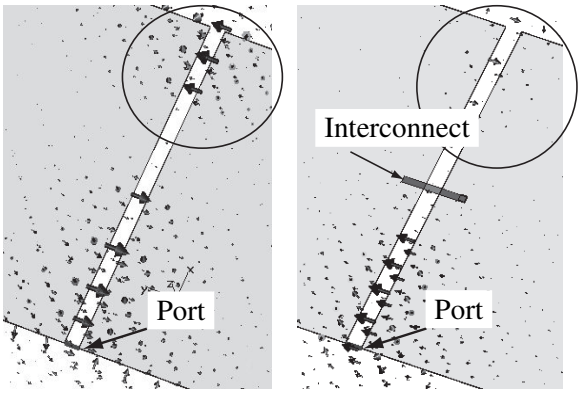

Fig. 9: Electric field distribution in the slot between the patches in the absence (a) and in the presence (b) of an interconnection wires.

We propose the introduction of a transformer to the feeding network of the antenna. By careful transformer design we can account both for the influence of the interconnects on the antenna return loss and for the coupling between the antenna and the cross-gap interconnects. A DC connection between the antenna electrodes, which is required for proper operation of the CMOS circuit, can also be achieved.

The schematic diagram of such a transformer is presented in Fig. 10. The transformer consists of three windings. The self-inductance of windings 2 and 3, as well as the mutual inductance between them, M_{23}, are very small for the operational

frequency of the CMOS circuit. The mutual inductance between windings 1 and 2, M_{12}, and between windings 1 and 3, M_{13}, are the same, i.e. $M_{12} = M_{13}$. Winding 2 connects output stage to an input stage. Winding 3 connects the local CMOS circuitry ground planes, denoted with GND1 and GND2, which are also the two antenna patches. Therefore windings 2 and 3 are a two-wire interconnection bus.

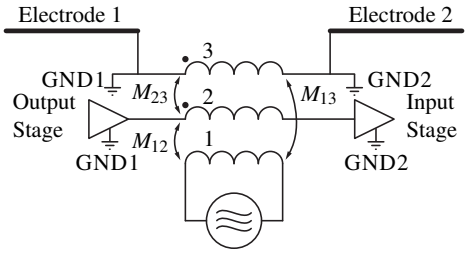

Fig. 10: Principle schematic of antenna feeding with transformer.

An RF signal is fed to winding 1. Due to the mutual inductance M_{13} the signal is coupled to winding 3, thus feeding the antenna. Since the mutual inductances M_{13} and M_{12} are equal, the RF voltage induced at the input of the input stage is the same as the RF voltage, induced at the reference ground of that stage, therefore there is no RF voltage drop at the input of the buffer. A possible realisation of the described transformer is shown in Fig.11. The simulated *S*-parameters of the transformer 4-port are presented in Fig.12.

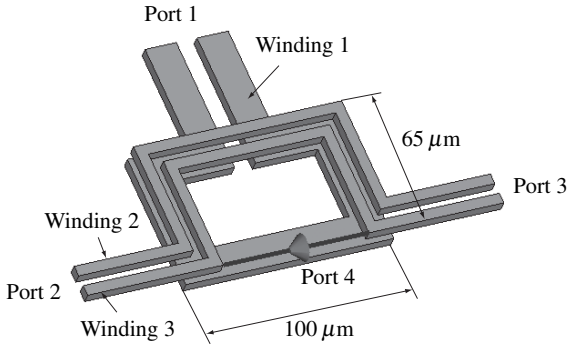

Fig. 11: Feeding transformer.

The presented structure is suitable for a single-wire interconnect. As normally parallel buses are used in the CMOS integrated circuits, more secondary windings can be introduced. For a N-wire bus $N+1$ secondary windings are required.

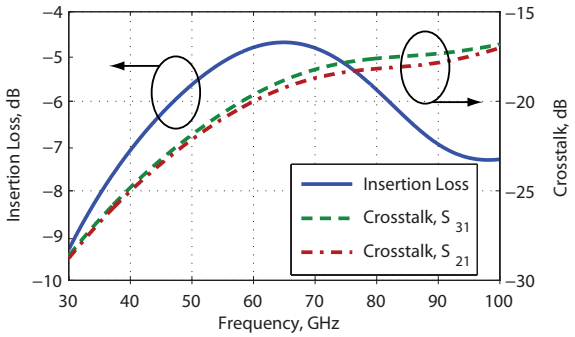

Fig. 12: Insertion loss and cross-talk coefficient between the antenna and the interconnects.

4 Conclusion

This work presents a novel approach for on-chip antenna integration, based on the cutting of the CMOS ground plane into patches and using the patches as antenna electrodes. The radiation characteristics of the antenna have been verified and the coupling between the antenna and the CMOS circuit has been reduced by including a transformer in the antenna feeding network.

Acknowledgment

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