

## Multiple-Valued CMOS Logic Circuits With High-Impedance Output State

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**Abstract:** Principles and possibilities of synthesis and design of bus interface circuits with high-impedance output state in multiple-valued logic systems are described and proposed in the paper. The general principles for implementation of such circuits are considered first. Then the methods for synthesis and design of logic circuits with high-impedance output state in multiple-valued CMOS logic systems with any logic basis are proposed and described. Two principles of synthesis and implementation of CMOS multiple-valued logic circuits with high-impedance output state are proposed and described: the simple circuits with smaller number of transistors, and the buffer/driver circuits with decreased propagation delay time. As an example, the schemes of such CMOS multiple-valued logic circuits with the logic basis of 5 (quinternary multiple-valued logic circuits) are given and analyzed by computer simulations. Some of computer simulation results confirming descriptions and conclusions are also given in the paper.

**Keywords:** Multiple-valued logic systems and circuits, bus interface circuits, high-impedance output state, CMOS logic circuits, quinternary multiple-valued logic circuits, synthesis and design, computer simulation.

### 1 Introduction

Digital systems that are practically in use are still binary digital systems. However, with rapid development of LSI and VLSI technologies, the possibilities and reasons for implementation of digital systems with the logic basis

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greater than 2 (multiple-valued or MV systems and logic) are becoming real and applicable in parts of a digital system[1-4].

Advantages and good characteristics of MV logic systems and circuits are created great interest for practical design and implementation of such systems and circuits [1-4]. There are many advantages of MV logic systems and circuits comparing with the binary ones. The main advantages of MV logic are: greater speed of arithmetic operations, greater density of memorized information, better usage of transmission paths, decreasing of interconnections complexity and interconnections area (both in the integrated circuit and in the system), decreasing of pin number of integrated circuits and printed boards, possibilities for easier testing of digital systems [1,2].

Practically, the greatest interest is for and the most investigated, developed and implemented are the ternary (with the logic basis of 3) and quaternary (with the logic basis of 4) MV circuits and systems [1-4]. The first investigated and practically implemented have been ternary MV circuits and systems. Later, the greatest practical interest is for investigation and application of quaternary logic systems and circuits. But, of course, it exists the interest for a general approach for synthesis, design and implementation of multiple-valued logic with any logic basis greater than 2.

The common buses are mainly used method for the data transmission in the binary digital systems. Connection to the buses is implemented by the logic circuits with high-impedance output state (three-state circuits). Because of the same reasons as in the binary systems, the common buses and the logic circuits with high-impedance output state are also used in the multiple-valued digital systems [1,2]. Of course, the MV digital signals are transmitted in such systems.

The reasons and advantages for application of CMOS technology in implementation of binary digital systems and circuits are very well known. All these good characteristics should be also kept in MV logic systems and circuits. There are also some advantages of CMOS technology that are important and characteristic for MV logic [1-4]. Also, since the first papers about MV logic circuits implementation, the greatest interest exists for implementation in CMOS technology. All these are the reasons that the CMOS technology is the most often used also for design and implementation of multiple-valued circuits and systems.

Possibilities and methods of synthesis and design of bus interface circuits with high-impedance output state in MV logic systems are considered in the paper. The general methods for design of such MV logic circuits are briefly described. Then methods for synthesis and design of CMOS MV

logic circuits with high-impedance output state are proposed and detailed described. Two principles of synthesis and implementation of CMOS MV logic circuits with high-impedance output state are proposed and described: the simple circuits with smaller number of transistors, and the buffer/driver circuits with decreased propagation delay time. The principal schemes for synthesis of such MV bus interface circuits are given and described firstly. Then, the described principles are illustrated and confirmed on an example of MV circuits with logic basis of 5 (quinternary logic circuits). The concrete schemes of such quinternary bus interface CMOS logic circuits with high-impedance output state are given and analyzed by computer simulations. All proposed principles and results have been analyzed and confirmed by PSPICE simulation for one CMOS technology process [5]. Some of computer simulation results confirming descriptions and conclusions are also given in the paper.

## 2 Multiple-Valued Bus Interface Circuits

The concept of common bus is very well known in binary digital systems. The common bus (or only bus) is a common two-way transmission path between all of more system units connected to the bus in the digital system. The bus consists of a set of parallel lines (wires) that parallel transmit the data between all units connected to the bus in the system. This technique greatly reduces system wiring by the sharing of common input/output lines of the bus. Because of the same reasons and advantages as in the binary systems, the buses are also used in the multiple-valued digital systems [1,2]. But, the multiple-valued digital signals are used and transmitted in such MV digital systems.

The special types of MV bus interface circuits are used for connection of system units to the bus. Since the bus is two-way path and the transmission is also two-way, there are two parts of such interface circuit. These parts are the input part and the output part, looking from the system unit side. One input/output two-way circuit is used for connection to each of bus lines. One such MV circuit is used for input/output transmission of one MV signal of data between each system unit and the bus. The principle schemes of such input/output bus interface circuits are shown in Fig.1. It is used  $n$  such interface circuits for the connection of one system unit to the bus, where  $n$  is number of bus lines and number of MV signals that are parallel transmitted between system unit and the bus. There are  $m$  such groups of  $n$  interface circuits from Fig.1 in the system with  $m$  units connected to the

bus. To enable two-way data transmission and the transmission between any pair of the units, the bus MV interface circuits are controlled by appropriate MV control signals. The control signals are generated by control logic. The control logic generates appropriate control signals on the basis of the signals from system units connected to the bus. To enable two-way data transmission the output circuits are circuits that can have high-impedance output state. So, such bus is bus with high-impedance state.

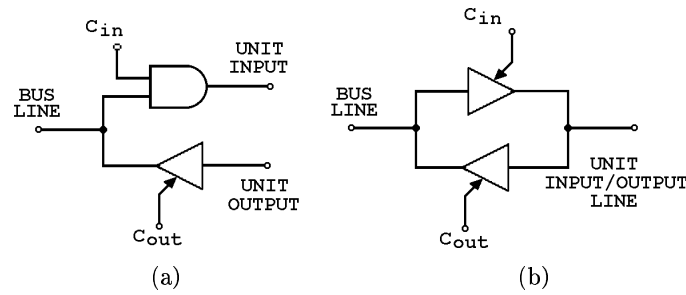


Fig. 1. Principle schemes of multiple-valued bus interface circuits.

The two schemes from Fig.1 are used depending on the structure of system units connected to the bus. When the unit has separated lines and structures for input and output of data then the circuit from Fig.1(a) is used (so called bus receiver/transmitter circuit). The circuit from Fig.1(b) (so called bus transceiver circuit) is used when the unit has common input/output lines and appropriate structures.

The bus interface circuits from Fig.1 consist of appropriate MV logic circuits. Input circuit in Fig.1(a) is two-input AND MV logic circuit. Output circuit in Fig.1(a) and both circuits in Fig.1(b) are MV logic circuits with high-impedance output state. Control signals  $C_{IN}$  and  $C_{OUT}$  enable input or output data transmission. For  $C_{IN} = K$  (where  $K$  is the highest logic state) and  $C_{OUT} = 0$  (where 0 is the lowest logic state) the input transmission is enabled. For  $C_{IN} = 0$  and  $C_{OUT} = K$  the output transmission is enabled. For  $C_{IN} = C_{OUT} = 0$  both input and output transmissions are disabled.

Principles of synthesis and design of AND CMOS MV logic circuits have been proposed and described in paper that has been describing the MV CMOS logic circuits [6]. It will be here in more details considered and proposed way of synthesis, design and realizations of CMOS MV bus interface circuits with high-impedance output state. Principles of synthesis and design of ternary and quaternary CMOS logic circuits with high-impedance output state have been proposed and described in papers that have been

published earlier [7,8]. It will be proposed and described here way for synthesis of electrical scheme and design of such circuits with any logic basis. Then, the proposed and described principles will be illustrated on example of synthesis and design of such quinary CMOS MV circuits. The proposed principles and the circuit schemes have been analyzed and confirmed by PSPICE simulation. Some of computer simulation results confirming descriptions and conclusions are given in the paper.

### 3 CMOS Multiple-Valued High-Impedance Output State Circuits

There are two methods to obtain high-impedance output state in the CMOS multiple-valued logic circuits. The first method uses CMOS transmission gate at the output of complete circuit. The second method uses principle of disconnecting the circuit output from the supply voltages.

Two types of CMOS multiple-valued and quinary circuits with high-impedance output state are considered, proposed and described here. The first type are the simple circuits with minimal number of transistors. The second type are the buffer/driver circuits with powerful output and decreased propagation delay time.

#### 3.1 Simple Circuits

The principle schemes of simple CMOS multiple-valued logic circuits with high-impedance output state are shown in Fig.2. The two possible methods for synthesis of simple circuits are shown in Fig.2.

The circuit in Fig.2(a) has the CMOS transmission gate (TG) at the output of standard CMOS multiple-valued identity logic circuit (MVIC). Standard CMOS binary inverter with supply voltages  $V_{SS}$  and  $V_{dd(K-1)}$  is used for control of CMOS transmission gate. For  $C = K$  transistors in transmission gate are turned on and then is  $Z = X$ . For  $C = 0$  transistors in transmission gate are turned off and the output of the circuit is in the high-impedance state.

The circuit in Fig.2(b) has additional transistors connected between standard CMOS multiple-valued identity logic circuit (MVIC) and the supply voltages. These serial transistors disconnect the circuit output from supply voltages in the high- impedance state. Standard CMOS binary inverter with supply voltages  $V_{SS}$  and  $V_{dd(K-1)}$  is used for control of additional CMOS transistors. For  $C = K$  all additional transistors are turned on and

then is  $Z = X$ . But, for  $C = 0$  all additional transistors are turned off and the circuit output is in the high-impedance state.

In Fig.2 MVIC is CMOS standard multiple-valued identity circuit with any logic basis and TG is standard CMOS transmission gate. Voltages  $V_{SS}$ ,  $V_{dd1}$ ,  $V_{dd2}$ ,  $V_{dd3}$ , and all up to  $V_{dd(K-1)}$  are supply voltages of the CMOS MV circuits, where  $V_{SS}$  is the lowest and  $V_{dd(K-1)}$  is the highest supply voltage.  $K$  is the logic basis and number of logic output states and number of supply voltages of the circuits.

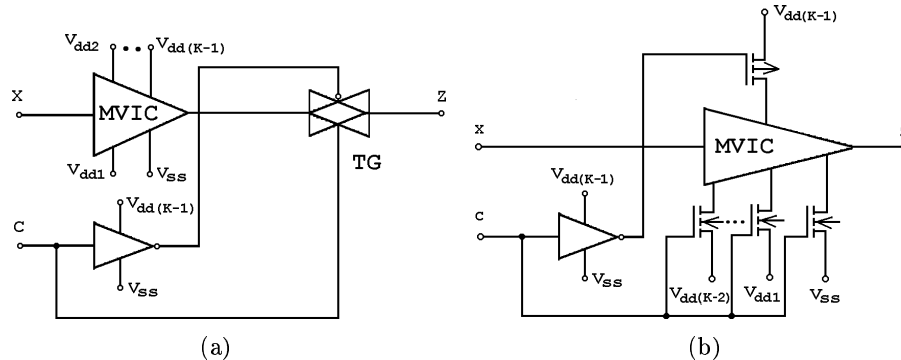


Fig. 2. Principle schemes of simple CMOS multiple-valued high-impedance output state circuits.

Principle schemes from Fig.2 can be used for synthesis of simple high-impedance output state CMOS circuits with any logic basis. As an example, it will be here shown a way for synthesis of such quinary circuits with logic basis of 5.

Schemes of the quinary simple circuits with minimal number of transistors, obtained on the principles shown in Fig.2., are proposed and given in Fig.3. These circuits use the standard CMOS inverters at the input. Circuit in Fig.3(a) has standard CMOS transmission gate at the output. The transmission gate is turned on for  $C = 4$  and turned off for  $C = 0$ . Circuit in Fig.3(b) has serial connection of MOS transistors at the output. This enables obtaining of high-impedance at the circuit output for  $C = 0$  when two of serially connected MOS transistors ( one NMOS and one PMOS transistor) are turned off. It can be seen from Fig.3(b) that the proposed circuit in Fig.3(b) is simpler than the circuit that can be obtained by direct applying of principle shown in Fig.2(b). Both circuits in Fig.3 use only two additional transistors comparing with standard CMOS quinary identity logic circuit. We here propose such way of synthesis of this type of simple circuit. It can be shown that such MV CMOS simple circuits for any MV logic ba-

sis can be obtained by adding only two CMOS transistors into scheme of standard CMOS MV identity logic circuit with the same MV logic basis. It can be seen from Fig.3 that both simple circuits have the same number of MOS transistors. But, circuit from Fig.3(a) has an advantage. It has smaller dynamic output impedance than the circuit in Fig.3(b).

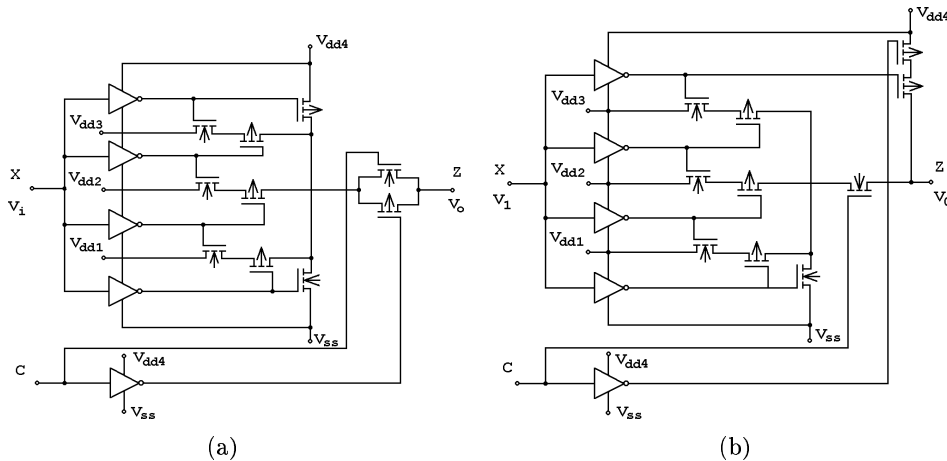


Fig. 3. Schemes of simple CMOS quinary high-impedance output state circuits.

Good characteristics of the simple circuits are minimal number of transistors and small propagation delay times when capacitive load of the circuit is small. The disadvantage is serial connection of more output MOS transistors, what produces greater propagation delay times when capacitive load of the circuit is greater.

Characteristics of the simple quinary CMOS high-impedance output state circuits from Fig.3 have been analyzed by PSPICE simulation. Some results of the PSPICE simulation of circuits from Fig.3 are given in Fig.4 and Fig.5. As an example, the circuits have been analyzed for situation when supply voltages are  $V_{SS} = 0V$ ,  $V_{dd1} = 3V$ ,  $V_{dd2} = 6V$ ,  $V_{dd3} = 9V$  and  $V_{dd4} = 12V$ , when the circuits are symmetrical and for one CMOS technology process [5].

The static voltage transfer characteristic for the circuit in Fig.3(a), obtained by simulation, when the output is enabled (for  $C = 4$  or for voltage  $V_{dd4}$  at input C) is given in Fig.4. It can be seen from Fig.4 that the circuit, as any quinary circuit, has five logic levels and four threshold voltages. The voltages of logic levels are equal to the voltage supplies. The threshold voltages depend on supply voltages and geometry of CMOS transistors. When the structure of circuit is symmetrical the threshold voltages are approxi-

mately at center between neighboring supply voltages. The static voltage transfer characteristic of circuit from Fig.3(b) for  $C = 4$  is very similar to the characteristic given in Fig.4.

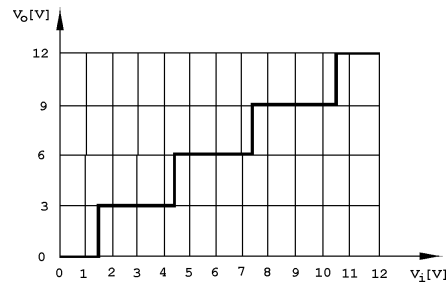


Fig. 4. Static voltage transfer characteristic of simple circuit from Fig.3(a).

Results of simulation of dynamic characteristics for circuit from Fig.3(a) are given in Fig.5. Two the most important dynamic characteristics have been analyzed: average propagation delay time and average propagation delay times for transition of circuit output to and from high-impedance state. Average propagation delay time as a function of capacitive load  $C_L$ , when the circuit output is enabled, is shown in Fig.5(a). Coefficient  $k_0$  in Fig.5(a) represents the power of output MOS transistors. It is ratio of power (geometry) of output transistors and standard transistors for used technology process. Average propagation delay times for the transition of circuit output to and from high-impedance state as a function of  $C_L$  are shown in Fig.5(b). In Fig.5(b) time  $t_{dSH}$  is average delay time of transition from some of static

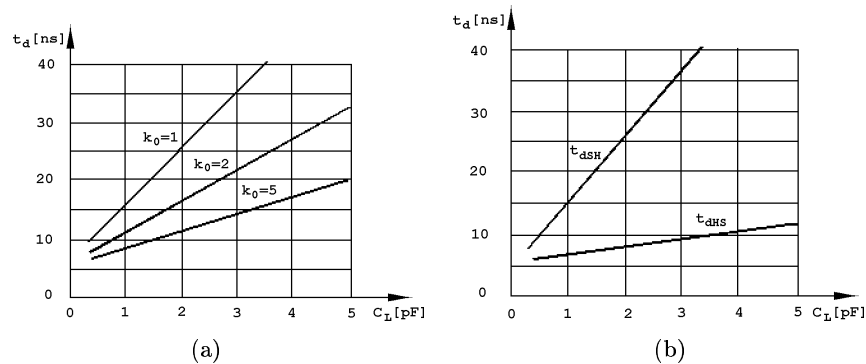


Fig. 5. Dynamic characteristics of simple circuit from Fig.3(a).

states to high-impedance state, and time  $t_{dHS}$  is average delay time for transition from high-impedance state to some of static states. Given results have



been obtained for the same supply voltages and the same CMOS technology process as for static voltage transfer characteristic and for  $R_L = 50k\Omega$ .

### 3.2 Buffer/Driver Circuits

Buffer/driver circuits should use schemes with minimal number of CMOS output transistors. The principle scheme for synthesis of CMOS multiple-valued buffer/driver circuits with high-impedance output state is proposed here and is shown in Fig.6. The output part of the circuit is similar as

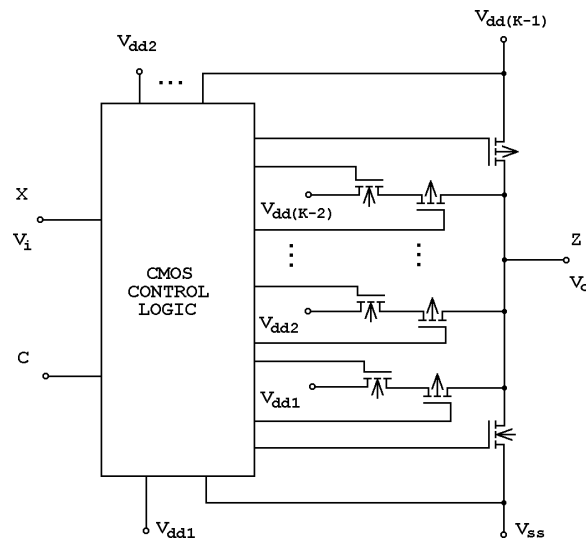


Fig. 6. Principle scheme of CMOS multiple-valued high-impedance output state buffer/driver circuit.

in standard CMOS multiple-valued circuits [6]. Appropriate CMOS control logic is used for control of circuit output CMOS transistors. This control logic turns on or turns off the output CMOS transistors depending on logic state at information input  $X$  and control input  $C$ . For  $C = 4$  the circuit works as the standard CMOS multiple-valued circuit and then is  $Z = X$ . For  $C = 0$  the output of the circuit is in high-impedance state. Needed output power is obtained by adequate design of output CMOS transistors only. This principle scheme of CMOS multiple-valued high-impedance output state circuit (Fig.6) can be used for synthesis of the circuit for any logic base  $K$ . If  $K$  is greater the output part of the circuit would have more pairs of serially connected CMOS transistors. In the circuit with basis of  $K$ , it is used  $(K - 2)$  pairs of serially connected CMOS transistors in the output

part of the circuit. Also, the CMOS control logic would be more complex if  $K$  is greater.

Principle schemes from Fig.6 can be used for synthesis of buffer/driver high-impedance output state CMOS circuits with any logic basis. As an example, it will be here proposed and shown a way for synthesis of such quinternary circuits with logic basis of 5.

It is possible to obtain different schemes of CMOS multiple-valued and also CMOS quinternary buffer/driver circuits on the basis of principle shown in Fig.6. Difference between possible solutions is in the way of realization of CMOS control logic. One possible solution, the circuit with control logic realized by standard binary CMOS NAND and NOR circuits and binary CMOS inverters is shown in Fig.7. For greater logic basis  $K$ , if  $K$  increases for 1, the CMOS control logic at circuit input will have one standard CMOS binary NAND circuit and two standard CMOS binary inverters more than for logic basis  $K$ .

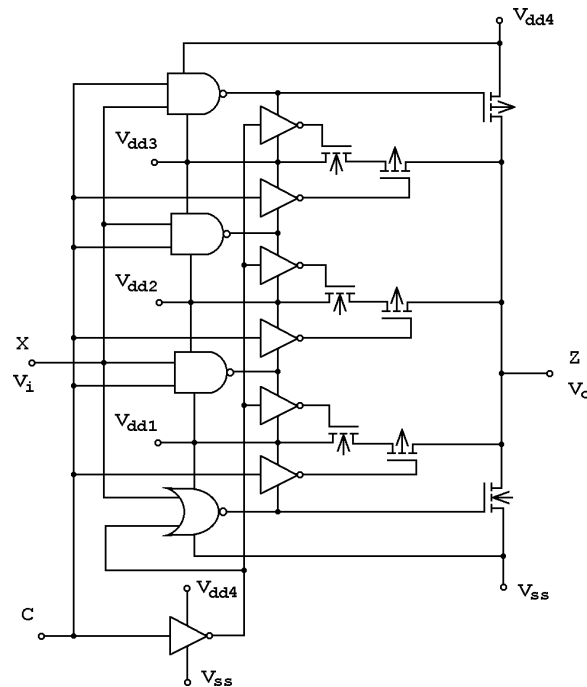


Fig. 7. One possibility of realization of CMOS quinternary high-impedance output state buffer/driver circuit.

However, the optimal CMOS quinternary high-impedance output state buffer/driver circuit, both by number of CMOS transistors and by working

speed, is shown in Fig.8. This circuit uses CMOS transistors network as the control logic for output transistors. This principle can be also used for synthesis of optimal such multiple-valued circuits with greater logic basis. If the logic basis  $K$  increases for 1, the CMOS control logic at circuit input will have six MOS transistors more than for basis  $K$ .

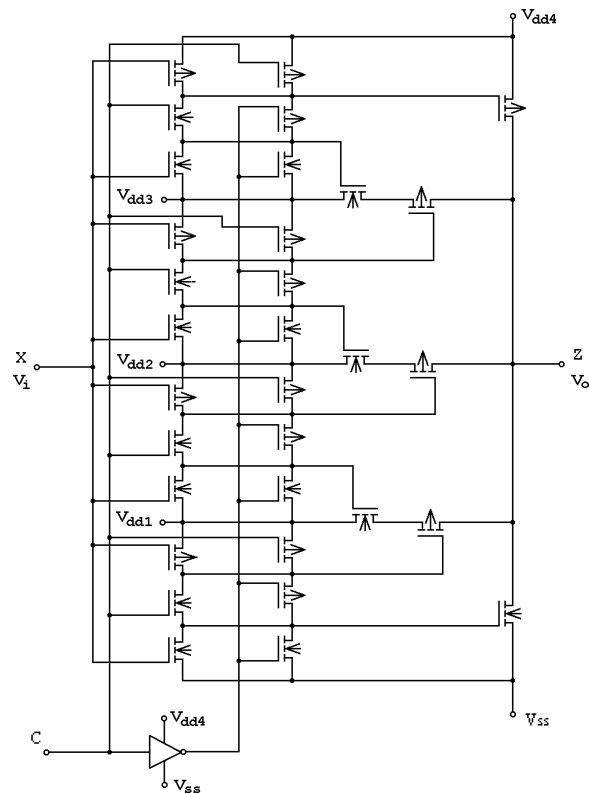


Fig. 8. Scheme of optimal CMOS quinary high-impedance output state buffer/driver circuit.

Characteristics of the quinary CMOS buffer/driver circuits with high-impedance output state have also been analyzed by PSPICE simulations. Some results of the simulation of optimal buffer/driver circuit from Fig.8 are given in Fig.9. The static voltage transfer characteristic for  $C = 4$  is very similar to the characteristic given in Fig.4. So, the dynamic characteristics are only shown here. Average propagation delay time as a function of  $C_L$  is shown in Fig.9(a). Average propagation delay times for the transition of circuit output to and from high-impedance state as a function of  $C_L$  are shown in Fig.9(b). Given results have been obtained for the same

conditions as the results for circuit in Fig.3(a) that are shown in Fig.4 and Fig.5.

The buffer/driver circuits are more complex, with more transistors, than the simple circuits. But, the buffer/driver circuits have greater output power and smaller propagation delay times when driving lines with heavy capacitive loads as the common bus lines are.

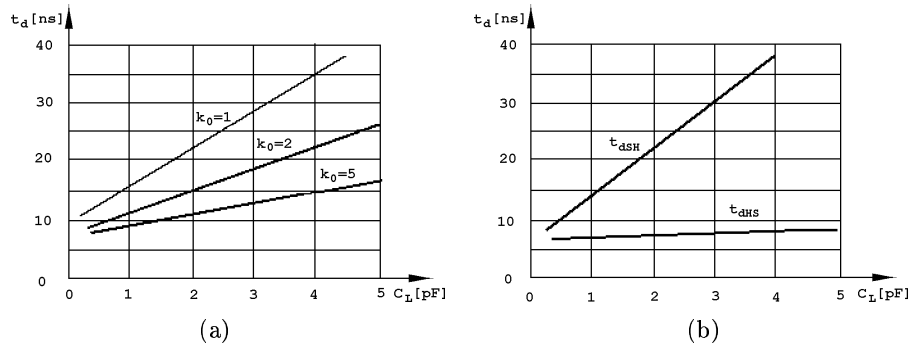


Fig. 9. Dynamic characteristics of buffer/driver circuit in Fig.8.

## 4 Conclusions

The common bus with high-impedance state is the most used also in multiple-valued CMOS digital electronic systems. The here proposed and described CMOS multiple-valued and quinary circuits with high-impedance output state are the parts of bus interface circuits. These proposed and described circuits are fully CMOS circuits, without static power consumption. The circuits can be easily synthesized and designed according to working conditions of the circuit.

Two types of proposed multiple-valued and quinary CMOS circuits with high-impedance output state are proposed and described. The simple circuits, comparing with the buffer/driver ones, have less number of transistors. But, these circuits have greater propagation delay time for greater capacitive loads, and the circuit area increases much more when the output driving capability increases. So, the simple circuits need to be used inside of LSI and VLSI circuits, at smaller working frequencies and small capacitive loads, in situations when the most important is to obtain high-impedance output state. The buffer/driver circuits need to be used at greater working frequencies and greater capacitive loads. The buffer/driver circuits can be used as input or output circuits of LSI and VLSI systems, or as integrated

circuits of smaller scale of integration for connection to quaternary buses (special separated multiple-valued bus interface circuits).

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