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Current Mode Approach: High Performance 0.35 μm CMOS Class AB Push-Pull Current Amplifier

Lyes Bouzerara and Mohand T. Belaroussi

Abstract: A very high bandwidth class AB (Push-Pull) current amplifier using the compensation resistor technique is presented and analyzed. Such technique stands as a powerful method of bandwidth enhancement for general circuits using CMOS current mirrors. The proposed bandwidth is enhanced from 675 MHz for the uncompensated current amplifier to 745MHz for the compensated one without affecting the current gain and other design parameters such as power consumption and output swing. The circuit exhibits a current gain of 20 dB and consumes 1.48 mW for $\pm$2.5V power supply voltage. All simulation results were performed using Hspice tool with 0.35μm CMOS TSMC parameters.

Keywords: Microelectronics, current mode, CMOS technology, analog integrated circuits, class AB amplifiers, compensation resistor technique.

1 Introduction

The tradition of implementing analog circuits by means of voltage amplifiers is almost as old as the concept of electronic circuit design. The integrated electronic circuit, however, is a relatively new concept. Furthermore, integrated electronic circuits have significantly different limitations and strengths to the conventional discrete electronic circuits have. Since the active devices in integrated circuits amplify current rather than voltage various current-mode circuit ideas have emerged after the introduction of the

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The authors are with Centre de Développment des Technologies Avancées, Microelectronics and Nanotechnologies Division Haouch Oukil, BP.17, 16303, Baba Hassen, Algiers, Algeria (e-mails bouzerara.lyes@lycos.com and mtbelaroussi@cdta.dz).

integrated circuit. Voltage and current modes are the two main access-key in investigating the analog world. Their dual nature can help efficiently in making a comprehensive analysis of the problem. But whether using, the voltage approach or the current one depends exclusively on the application domain and the intended objectives. Current amplifiers perform the same functions in the current domain that traditional amplifiers do in the voltage domain [1, 2, 3]. Currently, current amplifiers seem to be favorable from the point of view of both dynamic range and closed loop bandwidth [1, 4, 5]. In the design of very wide-bandwidth monolithic circuit, current amplifiers have an intrinsic advantage over voltage amplifiers. Since most of the parasitics associated with the monolithic devices are capacitive, the amplifier bandwidths can be improved, if most or all of the signal processing on the chip can be done in terms of current rather than voltage amplification, thus eliminating voltage swings across parasitic capacitances at circuit nodes. For example, as a current amplifier, the transistor is useful for frequencies up to its cut-off frequency f_T. However, the useful range of most voltage amplifiers is significantly below that because of the excessive phase shifts associated with the voltage transfer across a transistor at high frequencies. Therefore, to utilize the maximum frequency capability of a Metal Oxide Semiconductor (MOS) transistor, it is necessary to utilize it as a current rather than voltage, amplifier whenever possible. On the other hand, the implementation of a high performance class AB amplifier is a hard task, in order to preserve accuracy, linearity and low power consumption. Thanks to a continuing reduction of MOS transistor channel lengths, resulting in increasing transistor cut-off frequencies, modern Complementary Metal Oxide Semiconductor (CMOS) silicon processes offer transistors with a cut-off frequency in the order of several gigahertz. As a result, the CMOS technology becomes feasible for those wideband analog applications that were traditionally built with bipolar devices. In this article, a class AB current amplifier using the compensation resistor technique [6, 7, 8] is presented and analyzed.

2 An Overview of the Different Existing Feedforward Techniques

Some of the present non-feedback bandwidth enhancing techniques are: cascoding [9], C_c cancellation [10] and parasitic capacitance compensation [11] techniques. Cascode and C_c cancellation techniques prevent bandwidth reduction caused by "Miller effect". Parasitic capacitance compensation

is a technique for canceling undesired capacitors of an amplifier. A new bandwidth-enhancing technique [10] was applied on bipolar wideband amplifiers. In this technique, a capacitive feedback is used in analogy to resistive feedback amplifiers. As capacitive feedback does not lower gain, the technique does not trade off gain for bandwidth. In bipolar wideband amplifiers, the pole-splitting action is undesirable, and two classic techniques are mainly used in order to overcome this effect: the cascode and C_c cancellation techniques. In the cascode technique, one side of the capacitor C_μ [10] connected to the low gain point of the emitter of cascode transistor. In this way, the amount of feedback current is reduced very sharply and the effect of this capacitor is almost eliminated. In the C_c cancellation technique, the junction collector- base capacitances of dummy transistor are used in a cross-coupled way to neutralize the feedback action of the capacitor C_μ. In the classical version of this method, the parasitic collector-substrate capacitances of dummy transistors add to the output nodes and act as a burden on those points. For this reason, the C_c cancellation technique is usually less effective than the cascode technique. This feedback capacitance is based on proper positioning of amplifier poles and is equally applicable to low-gain as well as high-gain amplifiers.

Two another novel techniques for broad-banding the gain bandwidth-product (GBW) of CMOS folded-cascode amplifiers have been analyzed and presented [12]. In contrast with the conventional feedforward technique using an ac bypass capacitance, these new methods offer the advantage of precise cancellation of the pole-zero pair. Furthermore, the frequency at which the pole-zero cancellation occurs is higher than for the conventional feedforward method. Moreover the new techniques employed in [12], are able to reduce the phase dip, which is a measure of the mismatch between the pole-zero pair, to a very small value and even to zero. This is a considerable advantage over the conventional feedforward technique where a relatively large mismatch between the pole-zero pair continues to exist.

Different approaches for frequency compensation that were applied for low voltage and low power CMOS and bipolar operational amplifiers, have been treated and discussed [13]. A comparison of these techniques points out that for most general-purpose integrated amplifiers, Miller compensation is the preferred.

Another type of compensation has been applied for general CMOS circuits, which use current mirrors [7]. This one is called the resistive compensation technique, which consists to introduce a compensation resistor between the gates of the primary transistor pair of the current mirror. This

topology can lead to extend the bandwidth without distorting the DC characteristics of the original circuits, and without also sacrificing other design parameters such as output swing, large signal gain and power consumption. A similar compensation technique has been used as base resistor scaling in bipolar current mirrors, but not for bandwidth enhancement as in the case of [7].

3 Wideband Class AB (Push-Pull) Current Amplifier

The studied circuit is shown in Fig. 1, [6, 14]. It is divided into an upper amplifier UA, and a lower amplifier LA. Two current mirrors compose the upper amplifier: MP3, MP4 and MN1, MN2, with a unity current ratio. MP5 and MN10 have a larger aspect ratio to achieve current gain. The lower amplifier is structured in the same way by two current mirrors: MP6, MP7 and MN8, MN9 with also a unity current ratio. This configuration allows good ac amplification with very low input impedance and high accuracy.

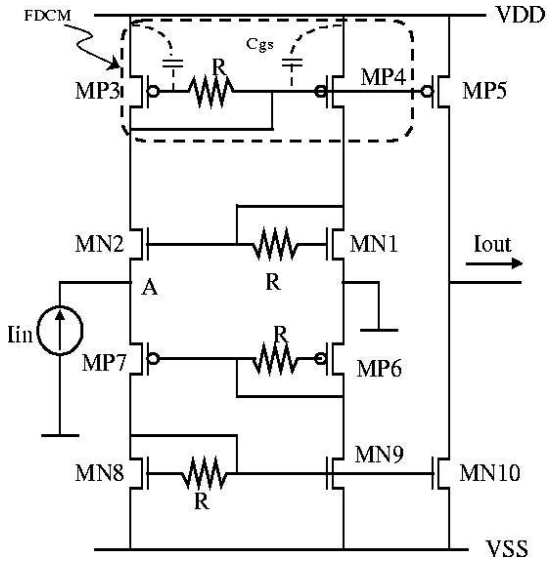

Fig. 1. CMOS Wideband Class AB (Push-Pull) Current Amplifier.

The current gain of the current amplifier is given by:

$$A_i = \frac{\left(\frac{W}{L}\right)_{MP5}}{\left(\frac{W}{L}\right)_{MP3}} = \frac{\left(\frac{W}{L}\right)_{MN10}}{\left(\frac{W}{L}\right)_{MN8}}, \tag{1}$$

where W is the channel width of a MOS transistor and L is the channel

length of a MOS transistor. This current gain is set by the aspect ratios of MP5 (MN10) and MP3 (MN8).

We used in this current amplifier, a simple but powerful technique of speed and bandwidth enhancement for CMOS current amplifiers [7, 8]. Introducing a compensation resistor between the gates and drains of the transistors of the current mirrors lead to a significant bandwidth enhancement.

As we know that current mirrors are one of the most indispensable building blocks of analog circuits, and especially in the current amplifiers circuits, thus the resistive compensation technique allows to improve the bandwidth of the current amplifier without distorting the dc characteristics of the original circuit. This resistor eventually delays the response but also introduces a zero, which cancels that delay.

As shown in Fig. 1 a resistor is connected between the drain and the gate nodes and forms a low pass filter (LPF) with a gate- source capacitance Cgs of the input transistor in the frequency dependent current mirrors (FDCM). For low frequencies and DC operations, the input impedance of the FDCM is low since the low frequency and DC components pass through the LPF. In this case the FDCM operates as a conventional current mirror. For frequencies higher than the cut-off frequency $1/(RC_{gs})$ of the LPF, the input impedance becomes higher since the drain-gate path is cut by the LPF and the input transistor of the current mirror operates like a current source. Introducing a compensation resistor in the current amplifier lead to a significant bandwidth enhancement. Due to the symmetry of the current amplifier, the transfer function is given for half of this circuit:

When the technique is not considered the transfer function in the Laplace domain is given by

$$H(s) = \frac{I_{out}}{I_{in}} = \frac{g_{m_5}}{g_{m_3}} \frac{1}{1 + \dfrac{C_{g_{s_4}} + C_{g_{s_5}}}{g_{m_3}} s}. \tag{2}$$

And thus the circuit bandwidth is: $\omega_{01} = g_{m_3}/(C_{g_{s_4}} + C_{g_{s_5}})$.

Adding the compensation resistor, the transfer function results now in:

$$H(s) = \frac{g_{m_5}}{C_{g_{s_4}} + C_{g_{s_5}}} \frac{s + \dfrac{1}{RC_{g_{s_3}}}}{s^2 + \dfrac{1}{RC_{g_{s_3}}} s + \dfrac{g_{m_3}}{RC_{g_{s_3}}(C_{g_{s_4}} + C_{g_{s_5}})}}. \tag{3}$$

In this case, the transfer function presents a zero and two poles, which

are given as follows:

$$z_1 = \frac{1}{RC_{g_{s_3}}} \tag{4}$$

$$p_{1,2} = \frac{1}{2RC_{g_{s_3}}}\Big[-1 \pm \sqrt{1 - \frac{4g_{m_3}RC_{g_{s_3}}}{(C_{g_{s_4}} + C_{g_{s_5}})}}\Big], \tag{5}$$

with a bandwidth of

$$\omega_{02} = \frac{1}{RC_{g_{s_3}}}\sqrt{1 - \frac{4g_{m_3}RC_{g_{s_3}}}{(C_{g_{s_4}} + C_{g_{s_5}})}}. \tag{6}$$

The frequency response determined by ω_{02} and ω_{01} for the compensated circuit and the uncompensated one, respectively, leads to the establishment of a ratio given by

$$\frac{\omega_{02}}{\omega_{01}} = \frac{1}{g_{m_3}RC_{g_{s_3}}}\sqrt{(C_{g_{s_4}} + C_{g_{s_5}})(C_{g_{s_4}} + C_{g_{s_5}} - 4g_{m_3}RC_{g_{s_3}})}. \tag{7}$$

The potential of the input node A of the circuit is, owing to the matching conditions in upper and lower amplifier, maintained at virtual ground both with and without ac input. And this condition is, to a first approximation, independent of the physical parameters (threshold voltage, transconductance etc.) of the pass transistors MN2 and MP7. For no ac input at the node A of the circuit, a quiescent current I_q flows in the two input paths and the product A_iI_q in the output path, thus $I_{out} = 0$. If input I_{in} is applied to the circuit, current variation Δi_1 and Δi_2 will occur in the input paths of upper and lower amplifier (push-pull operation), respectively.

The output current is given by

$$I_{out} = A_i(I_q + \Delta i_1) - A_i(I_q - \Delta i_2) = A_iI_{in}. \tag{8}$$

However, an accurate calculation of the quiescent current I_q is tedious, therefore, it can be approximately determined. Assuming that all transistors are operating in saturation, I_q may be expressed as

$$I_q \simeq \frac{1}{2}(I_{q_1} + I_{q_2}), \tag{9}$$

with

$$I_{q_1} = \frac{K_2K_3}{2(\sqrt{K_2} + \sqrt{K_3})^2}(V_{DD} - V_{T2} - |V_{T3}|)^2, \tag{10}$$

$$I_{q_1} = \frac{K_7K_8}{2(\sqrt{K_7} + \sqrt{K_8})^2}(|V_{SS}| - V_{T8} - |V_{T7}|)^2, \tag{11}$$

where K_i is the transconductance parameter of MOS transistor i, V_{Ti} is the threshold voltage of MOS transistor i, V_{DD} is the positive supply voltage, and V_{SS} is the negative supply voltage. I_{q_1} and I_{q_2} are quiescent currents in upper amplifier and lower amplifier respectively, if the input node A is short circuited to ground. We also have $I_{q_1} = I_{q_2}$ if $V_{DD} = V_{SS}$, all NMOS and PMOS transistors are identical (except for MP5 and MN10), and no body effect occurs.

The input impedance at this quiescent point is given by

$$Z_{in} = \frac{Z_{in_1} Z_{in_2}}{Z_{in_1} + Z_{in_2}}, \tag{12}$$

which is the input impedance of upper and lower amplifier in parallel. Assuming that $g_{m_i} \gg g_{d_i}$, we have

$$Z_{in_1} = \frac{1}{g_{m_2}} \left[\frac{g_{d_2} + g_{d_3}}{g_{m_3}} + \frac{g_{d_1} + g_{d_4}}{g_{m_1}} \right], \tag{13}$$

$$Z_{in_2} = \frac{1}{g_{m_7}} \left[\frac{g_{d_7} + g_{d_8}}{g_{m_8}} + \frac{g_{d_6} + g_{d_9}}{g_{m_6}(1 + \eta_6)} \right], \tag{14}$$

where $\eta_i = g_{mb_i}/g_{m_i}$, g_{d_i} is the drain conductance to V_{DS} of MOS transistor i, g_{m_i} is the transconductance to V_{GS} of MOS transistor i, and G_{mb_i} is the transconductance to V_{SB} caused by the body effect of transistor i.

The output impedance of the current amplifier is given by

$$Z_{out} = \frac{1}{g_{d_5} + g_{d_{10}}} \tag{15}$$

4 Simulation Results

In this section, we present Hspice simulation results. All of the simulations are based on twin-well *Taiwan Semiconductor Manufacturing Co (TSMC)* 0.35 μm CMOS process [15]. The dimensions of the transistors are as follows: $(W/L)_{MN10} = 200\ \mu/0.5\mu$ and $(W/L)_{MP5} = 200\ \mu/1\mu$ else $10\mu/0.5\mu$ for N-channel MOS transistors and $10\mu/1\mu$ for P-channel MOS devices. All NMOS bulks are connected to V_{SS} and all PMOS bulks are connected to V_{DD}.

The simulation results listed in the Table 2 show that the circuit exhibits a current gain of 20 dB and consumes 1.48mW for ±2.5 V power supply voltage. As summarized in the Table 1, the unity gain frequency is enhanced from 675 MHz to 745 MHz for different compensation resistor comprised

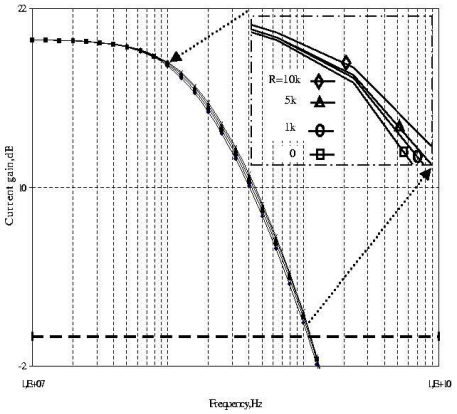

Fig. 2. Frequency response of the current amplifier for some compensation resistor values.

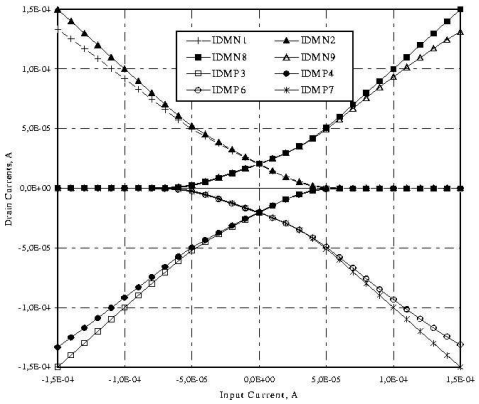

Fig. 3. Simulated drain currents of the transistors: MN1, MN2, MN8, MN9, MP3, MP4, MP6 and MP7.

between 0 and 10 kΩ; and this is illustrated in the Figure 2, which represents the frequency response of the current amplifier for some compensation resistor values. The simulated input and output impedances were 190 Ω and 150 kΩ respectively. For an input amplitude range of $-89\ \mu$A $\rightarrow +92\ \mu$A, all MOS transistors maintained strong inversion and the corresponding variation of the input voltage was from -13.38 mV to 29.48 mV.

Figure 3 illustrates the simulated drain currents of interest, which shows a quiescent current of 20 μA, and illustrates also a symmetry between the upper and the lower amplifier, which are in parallel.

Table 1. Unity gain frequency for different compensation resistor values.

Compensation resistor value	Unity gain frequency
0	675 MHz
500 Ω	680 MHz
1 kΩ	690 MHz
3 kΩ	705 MHz
5 kΩ	720 MHz
7 kΩ	730 MHz
10 kΩ	745 MHz

Table 2. Simulated performance characteristics of the current amplifier for ±2.5V power supply voltage.

Design parameters	Values
Technology	CMOS 0.35 μm
Current gain	20 dB
Quiescent current I_q	20 μA
Offset voltage (at $I_{in} = 0$)	3.46 mV
DC power dissipation	1.48 mW
Input impedance	190 Ω
Output impedance	150 kΩ
Input current range	-89 μA $\rightarrow$ 92 μA
Input voltage variation	-13.38 mV $\rightarrow$ 29.48 mV
Input voltage noise @ 1 GHz	25.72 pV/$\sqrt{\text{HZ}}$
Output voltage noise @ 1 GHz	1.75 nV/$\sqrt{\text{Hz}}$

5 Conclusion

For wideband current applications, current mirrors compensated with a resistor are advantageous to achieve high performance current amplifier. We used an elegant technique for improving current amplifier bandwidth. This technique improves the unity gain frequency of about 70 MHz when comparing the uncompensated circuit and the compensated one. Supported with Hspice simulations, this topology allows to extend the bandwidth without sacrificing other design parameters such as power consumption, output swing and the current gain. This technique seems to be useful in some applications such as industrial, biomedical and aerospace fields and many signal processing circuits, which use wideband current amplifiers.

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