Multiple-Valued Regenerative CMOS Logic Circuits With High-Impedance Output State

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Abstract: Principles and possibilities of synthesis and design of multiple-valued (MV) regenerative CMOS logic circuits with high-impedance output state and any logic basis are proposed and described in the paper. Two principles of synthesis and implementation of CMOS regenerative multiple-valued logic circuits with high-impedance output state are proposed and described: the simple circuits and the buffer/driver circuits. The schemes of such circuits are given and analyzed by computer simulations. Some of computer simulation results confirming descriptions and conclusions are also given in the paper.

Keywords: Multiple-valued logic systems and circuits, MV logic basis, CMOS logic circuits, regenerative logic circuits, high-impedance output state, logic schemes, synthesis and design, computer simulation, pSpice simulation.

1 Introduction

Digital logic systems that are practically in use are still binary ones. With rapid development of VLSI technologies, the possibilities for implementation of digital systems with the logic basis greater than 2 (multiple-valued or MV systems) are becoming real and applicable [1]-[4]. There are many advantages of MV logic comparing with the binary one creating great interest for implementation of such systems and circuits. The greatest interest is for investigation of ternary (logic basis

of 3) and quaternary (basis of 4) MV circuits and systems. But, there is interest for investigation and implementation of MV circuits and systems with any logic basis.

The common buses and logic circuits with high-impedance output state are mainly used for data transmission in the binary digital systems. Because of the same reasons as in the binary systems, the common buses and the logic circuits with high-impedance output state are also used in MV digital systems [1, 2]. There also exists the need for noise influence decreasing in such MV digital circuits and systems. So, there is need for using regenerative MV circuits with high-impedance output state. The advantages of application of CMOS technology in implementation of binary digital systems are very well known. Also, since the first MV logic circuits implementations, there is the greatest interest for implementation in CMOS technology [1]-[4].

Possibilities and methods of synthesis and design of MV regenerative CMOS logic circuits with high-impedance output state and any logic basis are considered in the paper. Two principles of synthesis and realization of such MV CMOS logic circuits are proposed and described: the simple circuits with smaller number of transistors, and the buffer/driver circuits with decreased propagation delay time. As an illustration of proposed methods, the concrete schemes of such quinternary (logic basis of 5) CMOS logic circuits are given. All proposed principles and circuits have been analyzed and confirmed by PSPICE simulation for one CMOS technology process [5].

2 Design Of MV Regenerative CMOS Logic Circuits With High-Impedance Output State

There are two methods to obtain high-impedance output state in CMOS MV logic circuits: using CMOS transmission gate at MV circuit output, or disconnecting MV circuit output from supply voltages. Realizations of CMOS MV circuits with high-impedance output state are proposed and described in paper [6]. Methods for obtaining of regenerative MV CMOS logic circuits are considered and described in paper [7].

2.1 Simple circuits

Principle scheme of simple MV CMOS regenerative circuits with high-impedance output state is shown in Fig. 1. The circuit has CMOS transmission gate (TG) at the output of regenerative MV CMOS circuit (RMVC) with any logic basis. Standard CMOS inverter is used for control of CMOS transmission gate. For $C = n - 1$ (n is used logic basis) transmission gate is turned on and $Z = X$. Then there is voltage histeresys in static voltage transfer characteristic. For $C = 0$ transmission gate is

off and output of the circuit is in the high-impedance state. Scheme of the simple quinternary circuit, obtained on the principles shown in Fig. 1, is proposed and given in Fig. 2. The circuit uses regenerative quinternary CMOS identity circuit at the input. Circuit in Fig. 2 has CMOS transmission gate at the output that is turned on for $C = 4$ and turned off for $C = 0$. The input regenerative quinternary CMOS identity circuit is obtained according to principles given in paper [7]. So, binary regenerative CMOS logic circuits are used at the input of circuits in Fig. 2. Binary regenerative CMOS circuits that are used here are proposed and described in paper [8]. Standard binary CMOS inverters in feedback loop give voltage histeresys in voltage transfer characteristic of the circuit.
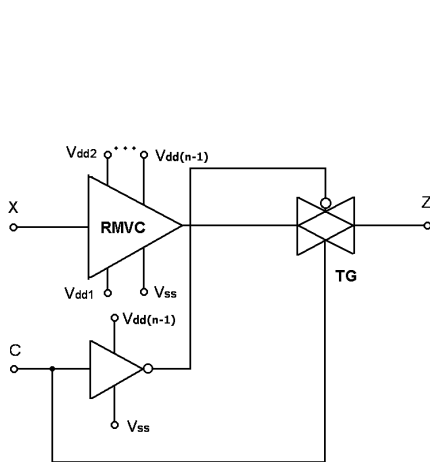
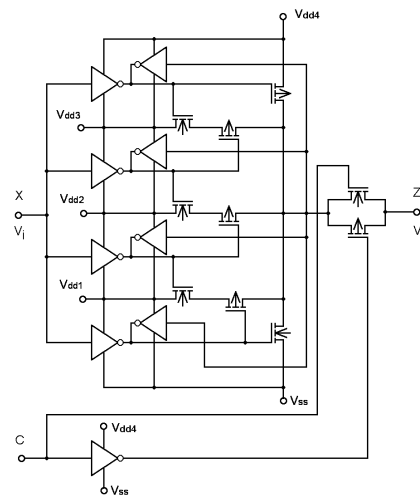Fig. 1. Principle scheme of simple MV circuit.

Fig. 2. Scheme of quinternary simple circuit.

Threshold voltages of the circuit can be obtained in the same way as for MV regenerative CMOS circuits or for binary CMOS regenerative circuits [7, 8]. It can be shown that the threshold voltages of the circuit are given by

$$V_{thi} = \frac{1}{2}[(2i-1)V_{dd} + V_h]$$
$$V_{tli} = \frac{1}{2}[(2i-1)V_{dd} - V_h]$$

(1)

where i is number of calculated voltage threshold. For logic basis of n value of i can be from 1 to $(n-1)$. For quinternary MV circuits value of i can be from 1 to

4. The voltage histeresys for any of change of input voltage is given by

$$V_h = V_{h1} = V_{h2} = \cdots = V_{h(n-1)} = \frac{V_{dd}(3V_{dd} - 4V_{th})}{4k(V_{dd} - 2V_{th})} \tag{2}$$

In the given equations k is ratio of transconductanse of input MOS transistors and MOS transistors in feedback loop. V_{tn} is threshold voltage of MOS transistors.

Dynamic characteristics depend on parameters of the circuit in the same way as for simple standard MV CMOS circuits with high-impedance output state [6].

2.2 Buffer/driver circuits

Buffer/driver circuits should use schemes with minimal number of CMOS output transistors. The principle scheme for synthesis of CMOS regenerative MV buffer/driver circuit with high-impedance output state and any logic basis is proposed and shown in Fig. 3. The output part is same as in standard CMOS MV circuits. Appropriate CMOS regenerative and control logic is used for control of circuit output transistors. This logic turns on or off the output CMOS transistors depending on logic state at information input X and control input C and gives histeresys in static voltage transfer characteristic of the circuit. For $C = n - 1$ the MV circuit works as standard CMOS regenerative MV circuit, $Z = X$ and exists voltage husteresys. For $C = 0$ the output of the circuit is in highimpedance state. Needed output power is obtained by adequate design of output CMOS transistors only.
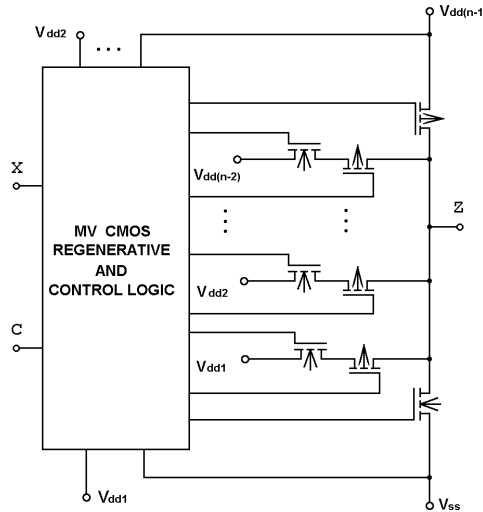

Fig. 3. Principle scheme of MV buffer/driver circuit.

It is possible to obtain different schemes of CMOS regenerative MV buffer/driver circuit on the basis of principle from Fig. 3. The difference between the solutions is in the way of realization of CMOS regenerative and control logic. As an example, the optimal quinternary buffer/driver CMOS regenerative high-impedance circuit both by number of transistors and by working speed is shown in Fig. 4. The circuit uses CMOS transistors network as the CMOS regenerative and control logic for output transistors. MOS transistors in feedback loop give histeresys in voltage transfer characteristic and increased noise immunity of the circuit.
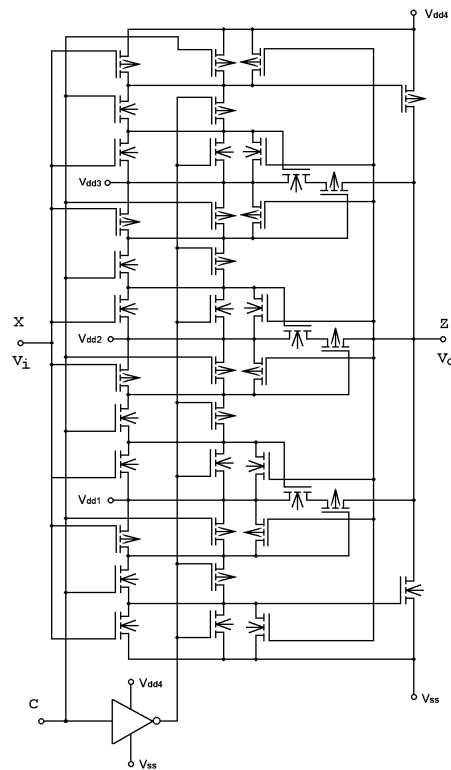

Fig. 4. Scheme of quinternary buffer/driver circuit.

Threshold voltages of the circuit can be obtained in the same way as for MV regenerative CMOS circuits or binary CMOS regenerative circuits. Given equations (1) and (2) can be used for calculation of threshold voltages. Dynamic characteristics depend on parameters of the circuit in the same way as for standard buffer/driver MV CMOS circuits with high-impedance output state [6].

2.3 Simulation results

Characteristics of proposed MV and quinternary circuits have been analyzed by PSPICE simulation. Simulation results confirmed given principles. Some results of simulation of circuits from Fig. 2 and Fig. 4 are given in Fig. 5 and Fig. 6. Static voltage transfer characteristic of the circuit from Fig. 2 for $C = 4$, obtained by simulation is shown in Fig. 5. Voltage transfer characteristic of circuit from Fig. 4 for $C = 4$ is practically the same as the characteristic given in Fig. 5.
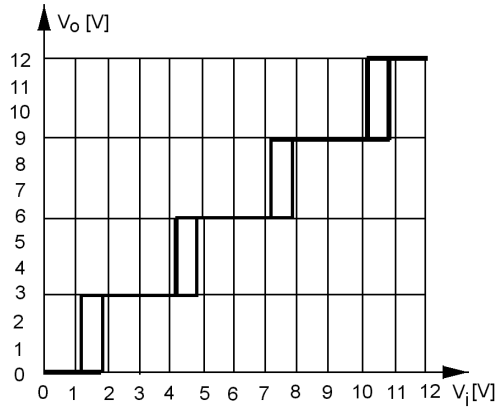

Fig. 5. Static voltage transfer characteristic of simple circuit in Fig. 2.

Results of dynamic characteristics simulation for circuits from Fig. 2 and Fig. 4 are given in Fig. 6. Average propagation delay times as a function of C_L are shown in Fig. 6a. Average propagation delay times for the transition of circuit output to and from high-impedance state as a function of C_L are shown in Fig. 6b. In Fig. 6b t_{dSH} is average delay time of transition from some of static states to high-impedance state, and t_{dHS} is average delay time for transition from high-impedance state to some of static states. Given results in Fig.5 and Fig. 6 have been obtained by simulation for $R_L = 50$ kΩ, for supply voltages $V_{SS} = 0$ V, $V_{dd1} = 3$ V, $V_{dd2} = 6$ V, $V_{dd3} = 9$ V, $V_{dd4} = 12$ V when the circuits are symmetrical and for one CMOS technology process [5]. Results for simple circuit in Fig. 2 are given with dashed lines and results for buffer/driver circuit in Fig. 4 are given and with full lines.

3 Conclusions

Here proposed principles and solutions give possibility to obtain and design MV regenerative CMOS circuits with high-impedance output state and any logic basis. The circuits have increased noise immunity and are fully CMOS circuits, without
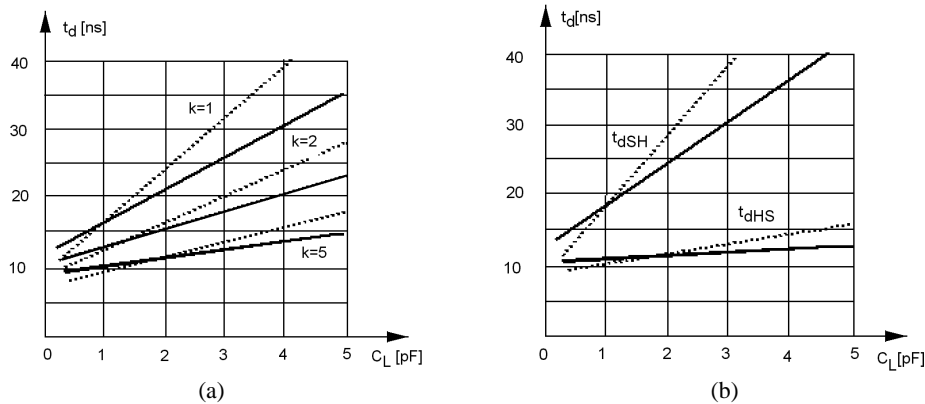
Fig. 6. Dynamic characteristics of circuits in Fig.2 and Fig.4.

static power consumption. The circuits can be easily synthesized and designed according to working conditions of the circuit.

The simple circuits, comparing with the buffer/driver ones, have smaller number of transistors. Disadvantage is serial connection of output MOS transistors. So, these circuits have greater propagation delay time for greater capacitive loads, and the circuit area increases much more when the output driving capability increases. The simple circuits need to be used inside of LSI and VLSI MV circuits and systems, at smaller working frequencies and small capacitive loads, in situations when it is important to obtain high-impedance output state and increased noise immunity. The buffer/driver circuits are more complex than the simple circuits. But, that circuits have greater output power and smaller propagation delay times when driving lines with heavy capacitive loads as the common bus lines are. The buffer/driver circuits have to be used at greater working frequencies and greater capacitive loads.

The buffer/driver circuits can be used as input or output circuits of LSI and VLSI MV circuits and systems, or as integrated circuits of smaller scale of integration for connection to MV buses (separated MV bus interface circuits).

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